

1 CLAIMS:

2 1. A method of depositing an aluminum nitride comprising layer
3 over a semiconductor substrate comprising:

4 positioning a semiconductor substrate within a chemical vapor
5 deposition reactor; and

6 feeding ammonia and at least one compound of the formula R_3Al ,
7 where "R" is an alkyl group or a mixture of alkyl groups, to the
8 reactor while the substrate is at a temperature of about 500°C or less
9 and at a reactor pressure from about 100 mTorr to about 725 Torr
10 effective to deposit a layer comprising aluminum nitride over the
11 substrate at such temperature and reactor pressure.

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13 2. The method of claim 1 wherein substrate temperature and
14 reactor pressure are maintained substantially constant during the feeding
15 and deposit.

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17 3. The method of claim 1 wherein substrate temperature is
18 greater than or equal to about 250°C during the feeding.

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20 4. The method of claim 1 wherein substrate temperature is
21 from about 380°C to about 420°C during the feeding.

22
23 5. The method of claim 1 wherein the aluminum nitride is
24 substantially amorphous.

1 6. The method of claim 1 wherein the reactor is void of
2 plasma during the depositing.

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4 7. The method of claim 1 wherein the compound comprises
5 triethylaluminum.

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7 8. The method of claim 1 wherein the compound comprises
8 trimethylaluminum.

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10 9. The method of claim 1 wherein the compound comprises at
11 least two different alkyl groups.

12
13 10. The method of claim 1 wherein the compound comprises at
14 least one methyl group and at least one ethyl group.

11. A method of forming DRAM circuitry comprising:
1 forming a first capacitor electrode over a substrate;
2 feeding ammonia and at least one compound of the formula R_3Al ,
3 where "R" is an alkyl group or a mixture of alkyl groups, to a
4 chemical vapor deposition reactor within which the substrate is received
5 while at a temperature of about 500°C or less and at a reactor
6 pressure from about 100 mTorr to about 725 Torr effective to deposit
7 a capacitor dielectric layer comprising aluminum nitride over the first
8 capacitor electrode;

10 forming a second capacitor electrode over the aluminum nitride
11 comprising capacitor dielectric layer; and

12 providing a DRAM word line comprising a gate of a field effect
13 transistor which has a pair of source/drain regions, one of the
14 source/drain regions being provided in electrical connection with the first
15 capacitor electrode, the other of the source drain regions being provided
16 in electrical connection with a DRAM bit line.

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18 12. The method of claim 11 wherein the compound comprises
19 triethylaluminum.

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21 13. The method of claim 11 wherein the compound comprises
22 trimethylaluminum.

1 14. The method of claim 11 wherein the compound comprises
2 at least two different alkyl groups.

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4 15. The method of claim 11 wherein the compound comprises
5 at least one methyl group and at least one ethyl group.

6
7 16. The method of claim 11 wherein substrate temperature is
8 greater than or equal to about 250°C during the feeding.

9
10 17. The method of claim 11 wherein substrate temperature is
11 from about 380°C to about 420°C during the feeding.

12
13 18. The method of claim 11 wherein substrate temperature and
14 reactor pressure are maintained substantially constant during the feeding
15 and deposit.

16
17 19. The method of claim 11 wherein the aluminum nitride is
18 substantially amorphous.

19
20 20. The method of claim 11 wherein the reactor is void of
21 plasma during the depositing.

1 21. DRAM circuitry comprising:

2 an array of word lines forming gates of field effect transistors and
3 an array of bit lines, individual field effect transistors comprising a pair
4 of source/drain regions; and

5 a plurality of memory cell storage capacitors associated with the
6 field effect transistors, individual storage capacitors comprising a first
7 capacitor electrode in electrical connection with one of a pair of
8 source/drain regions of one of the field effect transistors and a second
9 capacitor electrode, a capacitor dielectric region received intermediate
10 the first and second capacitor electrodes, the region comprising
11 aluminum nitride, the other of the pair of source/drain regions of the
12 one field effect transistor being in electrical connection with one of the
13 bit lines.

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15 22. The circuitry of claim 21 wherein the region contacts each
16 of the first and second capacitor electrodes and consists essentially of
17 aluminum nitride.

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19 23. The circuitry of claim 21 wherein the region contacts each
20 of the first and second capacitor electrodes and consists essentially of
21 aluminum nitride and native oxide formed on at least one of the first
22 and second capacitor electrodes.

1 24. The circuitry of claim 21 wherein the region contacts each
2 of the first and second capacitor electrodes and has a thickness less
3 than or equal to 60 Angstroms.

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5 25. The circuitry of claim 21 wherein the region contacts each
6 of the first and second capacitor electrodes and has a thickness less
7 than or equal to 50 Angstroms.

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9 26. The circuitry of claim 21 wherein the region contacts each
10 of the first and second capacitor electrodes, consists essentially of
11 aluminum nitride, and has a thickness less than or equal to 60
12 Angstroms.

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14 27. The circuitry of claim 21 wherein the region contacts each
15 of the first and second capacitor electrodes, consists essentially of
16 aluminum nitride and native oxide formed on at least one of the first
17 and second capacitor electrodes, and has a thickness less than or equal
18 to 60 Angstroms.

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20 28. The circuitry of claim 21 wherein the aluminum nitride is
21 substantially amorphous.

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1 29. A method of forming a field emission device comprising:
2 forming an electron emission substrate comprising emitters;
3 providing the emission substrate within a chemical vapor deposition
4 reactor;

5 feeding ammonia and at least one compound of the formula R_3Al ,
6 where "R" is an alkyl group or a mixture of alkyl groups, to the
7 reactor while the electron emission substrate is at a temperature of
8 about 500°C or less and at a reactor pressure from about 100 mTorr
9 to about 725 Torr effective to deposit a layer comprising aluminum
10 nitride over at least a portion of the emitters; and

11 after the deposit, joining the electron emission substrate with an
12 electron collector substrate.

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14 30. The method of claim 29 wherein the electron collector
15 substrate comprises a face plate comprising phosphor, and comprising
16 forming the device to comprise a field emission display.

17
18 31. The method of claim 29 wherein the electron emission
19 substrate comprises a conductive extraction grid formed outwardly of and
20 spaced from the emitters, the deposit occurring after formation of the
21 extraction grid.

1 32. The method of claim 29 wherein the electron emission
2 substrate comprises a conductive extraction grid formed outwardly of and
3 spaced from the emitters, the deposit occurring after formation of the
4 extraction grid and also occurring on the extraction grid.

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6 33. The method of claim 29 wherein the compound comprises
7 triethylaluminum.

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9 34. The method of claim 29 wherein the compound comprises
10 trimethylaluminum.

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12 35. The method of claim 29 wherein the compound comprises
13 at least two different alkyl groups.

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15 36. The method of claim 29 wherein the compound comprises
16 at least one methyl group and at least one ethyl group.

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18 37. The method of claim 29 wherein electron emission substrate
19 temperature is greater than or equal to about 250°C during the feeding.

20
21 38. The method of claim 29 wherein electron emission substrate
22 temperature is from about 380°C to about 420°C during the feeding.

1 39. The method of claim 29 wherein electron emission substrate
2 temperature and reactor pressure are maintained substantially constant
3 during the feeding and deposit.

5 40. The method of claim 29 wherein the aluminum nitride is
6 substantially amorphous.

8 41. The method of claim 29 wherein the reactor is void of
9 plasma during the depositing.

11 42. A field emission device comprising:
12 an electron emitter substrate comprising emitters having at least
13 a partial covering comprising aluminum nitride; and
14 an electrode collector substrate spaced from the electron emitter
15 substrate.

17 43. The field emission device of claim 42 wherein the electron
18 collector substrate comprises a face plate comprising phosphor, and the
19 field emission device comprises a field emission display.

21 44. The field emission device of claim 42 wherein the electron
22 emission substrate comprises a conductive extraction grid formed
23 outwardly of and spaced from the emitters, the covering being received
24 over the extraction grid.

1 45. The field emission device of claim 42 wherein the electron
2 emission substrate comprises a conductive extraction grid formed
3 outwardly of and spaced from the emitters, aluminum nitride of the
4 covering being in contact with the extraction grid.

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6 46. The field emission device of claim 42 wherein the emitter
7 covering consists essentially of aluminum nitride.

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9 47. The field emission device of claim 42 wherein the emitter
10 covering is void of oxide.

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12 48. The field emission device of claim 42 wherein the aluminum
13 nitride is substantially amorphous.

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15 49. The field emission device of claim 42 wherein the covering
16 comprises a thickness less than or equal to about 150 Angstroms.

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18 50. The field emission device of claim 42 wherein the covering
19 comprises a thickness greater than or equal to about 50 Angstroms.

1 51. A field emission device comprising:

2 an electron emitter substrate comprising emitters having at least
3 a partial covering comprising an electrically insulative material other
4 than an oxide of silicon; and

5 an electrode collector substrate spaced from the electron emitter
6 substrate.

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8 52. The field emission device of claim 51 wherein the electron
9 collector substrate comprises a face plate comprising phosphor, and the
10 field emission device comprises a field emission display.

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12 53. The field emission device of claim 51 wherein the electron
13 emission substrate comprises a conductive extraction grid formed
14 outwardly of and spaced from the emitters, the covering being received
15 over the extraction grid.

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17 54. The field emission device of claim 51 wherein the electron
18 emission substrate comprises a conductive extraction grid formed
19 outwardly of and spaced from the emitters, aluminum nitride of the
20 covering being in contact with the extraction grid.

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22 55. The field emission device of claim 51 wherein the covering
23 comprises a thickness less than or equal to about 150 Angstroms.

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2 56. The field emission device of claim 51 wherein the covering
comprises a thickness greater than or equal to about 50 Angstroms.
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